8.7 A Storage- and Power-Efficient Range-Matching TCAM for Packet Classification

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TCAMs utilize storage inefficiently in representing a range such as the TCP port field for packet classification, because they only allow exact match and mask operators [1]. TCAMs also consume a lot of power in their search lines since they are highly capacitive nodes subject to a full signal swing.

To solve these problems, the use of a range-matching cell (RMC) with a static match line and a charge-recycling technique in search lines is proposed. The proposed RMC offers range operators such as "Greater Than" in addition to "Equal", which increase the storage efficiency by up to 2.5 times compared with conventional TCAMs under typical packet classification rule sets [2]. In addition, the charge-recycling technique, commonly used in DRAM BLs, reduces the search-line power consumption by up to 60% compared with conventional precharged TCAMs. A 512×144b prototype chip, implemented using a 1.2V 0.13μm CMOS process, achieves a 4.8ns match cycle time with an energy efficiency of 0.59fJ/b/search.

Figure 8.7.1 shows a block diagram of the proposed TCAM, consisting of TCAM cells (TCCs), RMCs, and a priority encoder with association logic. To save power, entries in the sub-matching block (SMB) and the range-matching block (RMB) are enabled only when the 8b main matching block (MMB) has found a match. The MMB and RMB do not use the charge-recycling technique for a faster operation since the recycling incurs a delay in the charge recycling driver. The MMB and SMB use static TCCs that provide an exact match under arbitrary mask operations [1] for the longest prefix match required in searching the IP address field. The RMB uses RMCs specialized for range matching, which is applied on the two 16b port fields in the packet. When the range-matching rule includes two inequalities, such as A<Port<B, the association logic combines two neighboring entries to achieve a logical AND operation for the two inequalities. Such a combination is indicated by the association control cell (ACC) being set. Otherwise, entries are independently matched. A valid (VLD) cell in the MMB indicates the validity of the entry. An invalid entry is detected in the first stage of the search operation and the entire entry is deactivated all the way to the last stage to save power. The RMB keeps a 2b operator cell (OC) for each 16b RMC, and the OC indicates the type of operator to apply to the search data.

Even though 12.5% more transistors are used in the proposed RMC than in a conventional TCC, the RMC increases storage efficiency for typical L4 packet classification rules with ranges. Also, the RMC uses 43.8% less transistors than that of prior-art extended TCAM [2]. To store such a classification rule, conventional TCAMs expand the range with multiple entries. For example, a port range of 1024 to 65535 in both the source and destination port field occupies 36 entries in a conventional TCAM [2]. However, only one entry is required to represent the same port range in the proposed range-matching TCAM. Figure 8.7.2 shows how the entries are stored. The storage efficiency of the proposed TCAM can be increased up to 84% in a real router with typical rules, which is 2.5 times greater than that of a conventional TCAM, as shown in Fig. 8.7.2 [2].

Figure 8.7.3 shows an example of a 4b range-matching operation and the table of matching results used by the RMC. Range matching is done by bit-by-bit comparison, starting from the MSB to the LSB. The RMC pulls up (PU) or down (PD) its right-match line (RML) node, or passes (PASS) the decision of the left-match line (LML) node to the RML node depending on the evaluation result. For example, when the stored operator is "Greater than or Equal (GE)", the stored rule data is 1010, and the search data is 1100, then the first RMC from the MSB passes its decision to the next and the second RMC pulls down the match line to indicate a match, as shown in Fig 8.7.3. The results from the rest of the RMCs are overridden.

Figure 8.7.4 shows the circuit implementation and the WL structure of the proposed RMCs with a static match line. Each RMC is composed of a NAND-type cell to store one bit of rule data and a comparator. The OP0, OP1 and OP0+OP1 signals come from the OC shared by all RMCs in the same entry. When a bit of the stored rule data equals that of the search data, the match line transistor (MLT) is turned on and the range-comparing transistor (RCT) and the pull-up transistor (PT) are turned off, thereby connecting the RML node to the LML. When a bit of the stored rule data does not equal the bit of the search data, the RML node is pulled up if the stored operator is "Equal", otherwise it is pulled up or down depending on the match result.

A charge-recycling technique using a static TCC (STCC) is proposed to reduce the search-line power. Conventional TCAMs consume a lot of power in their search lines since these highly capacitive lines require transitions at every lookup cycle to precharge the match line [3]. To reduce the search-line power, the prior-art pulsed NAND-NOR CAM (PNN-CAM) [4] with a replica cell uses a charge-recycling driver with the dynamic match line. However, the STCC of the proposed TCAM does not require match-line precharging, thereby reducing the power consumption further. The STCC pulls up or down its match line depending on its match result, as shown in Fig. 8.7.5. Only when the search data changes, the charge-recycling driver draws current from the supply after recycling, as shown in the timing diagram of Fig. 8.7.5. Assuming that the transition probability of the search line is 0.5, the power consumption of the search line driver is reduced to 40% of that of a conventional precharged TCAM [3] including the control overhead of the charge-recycling driver.

The prototype chip is fabricated using a 0.13μm CMOS process. It occupies a chip area of 1.5×1.7mm^2. The proposed range-matching TCAM increases the storage efficiency by up to 2.5 times, compared with a conventional TCAM. Using the charge-recycling technique, the search-line power is reduced to 40% of that of the precharged TCAM [3]. The prototype chip achieves a 4.8ns search time and 1.46fJ/b/search energy. However, including the effect of the enhanced storage efficiency, the normalized energy is 0.59fJ/b/search, which shows at least twice the efficiency of other architectures, as shown in Fig. 8.7.6.

References:

[1] Huan Liu, "Efficient Mapping of Range Classifier into Ternary-CAM," *Proceedings of High Performance Interconnects,* pp. 95-100, Aug., 2002.

[2] E. Spitznagel, et al., "Packet Classification Using Extended TCAMs," *Proceedings of IEEE International Conference on Network Protocols*, pp. 120-131, Nov., 2003.

[3] I. Arsovski, et al., "A Mismatch-Dependent Power Allocation Technique for Match-Line Sensing in Content-Addressable Memories," *IEEE J. Solid-State Circuits,* vol. 38, no. 11, pp. 1958-1966, Nov., 2003.

[4] Byung-Do Yang et al., "A Low-Power CAM Using Pulsed NAND-NOR Match-Line and Charge-Recycling Search-Line Driver" *IEEE J. Solid-State Circuits,* vol. 40, no. 8, pp. 1736-1744, Aug., 2005.

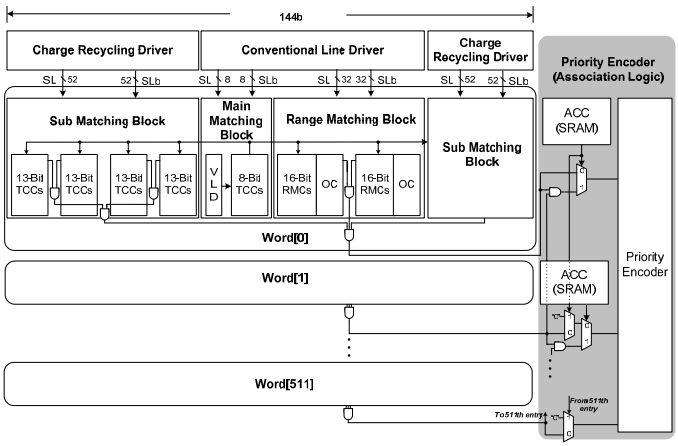

Figure 8.7.1: Block diagram of the implemented TCAM.

Case	Conventional TCAM		Proposed range-matching TCAM	
	Source Port Field(SP)	Destination Port Field(DP)	Source Port Field(SP)	Destination Port Field(DP)
1023 < (SP,DP)	1xxx xxxx xxxx xxxx 01xx xxxx xxxx xxxx 001x xxxx xxxx xxxx 0001 xxxx xxxx xxxx 0000 1xxx xxxx xxxx 0000 01xx xxxx xxxx	1xxx xxxx xxxx xxxx 01xx xxxx xxxx xxxx 001x xxxx xxxx xxxx 0001 xxxx xxxx xxxx 0000 1xxx xxxx xxxx 0000 01xx xxxx xxxx	0000 0100 0000 0000 OC : GE	0000 0100 0000 0000 OC : GE
	36 entries are occupied		(1 entry + 2 OCs) are occupied	

Example of range mapping on the TCAM for the case (SP,DP) > 1023

Rule Set	Rules	With ranges	TCAM Entries (conventional)	Storage efficiency (conventional)	TCAM Entries (Proposed)	Storage efficiency (Proposed)
1	279	26	949	29%	**302**	**92%**
2	183	24	553	33%	**207**	**88%**
3	68	12	128	53%	**80**	**85%**
4	158	10	418	37%	**168**	**94%**
5	264	176	1638	16%	**440**	**60%**
Avg	190	50	737	34%	**239**	**84%**

Storage efficiency of the proposed TCAM compared with conventional TCAMs

Figure 8.7.2: Range mapping and storage efficiency.

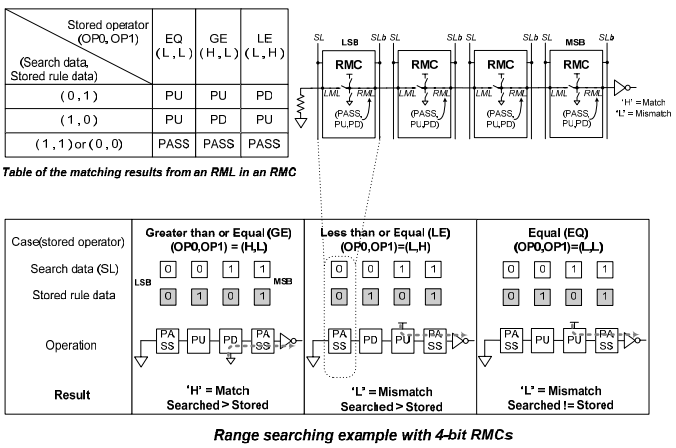

Figure 8.7.3: Matching results from an RMC and example of range searching.

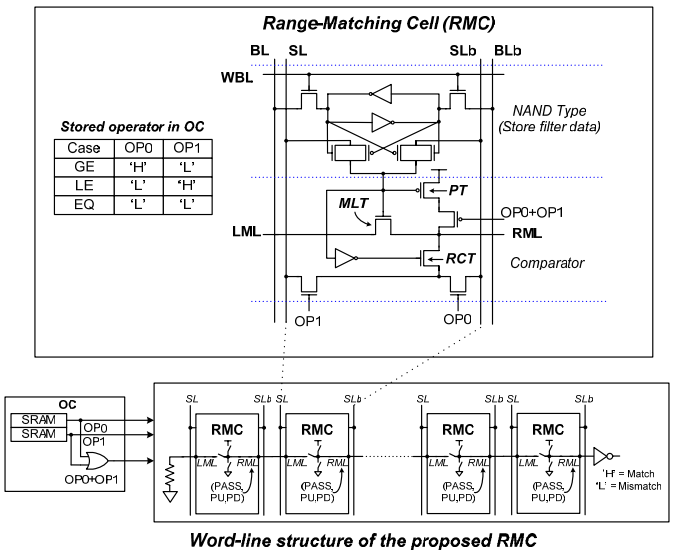

Figure 8.7.4: Proposed range-matching cell and its WL structure.

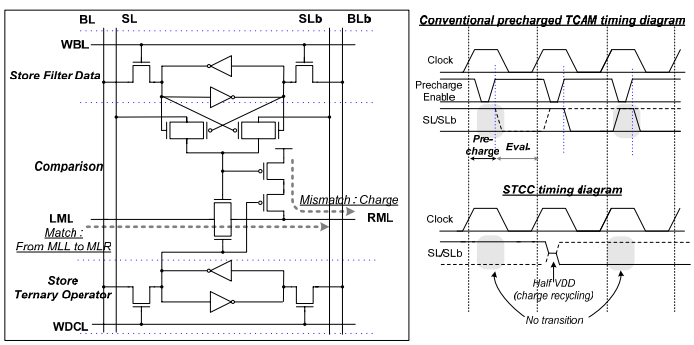

Figure 8.7.5: The proposed STCC and the timing diagram of the search line.

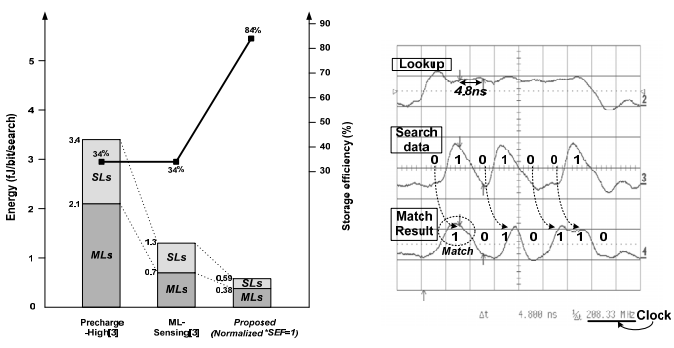

Figure 8.7.6: Power-and storage-efficiency comparison and measured waveform.

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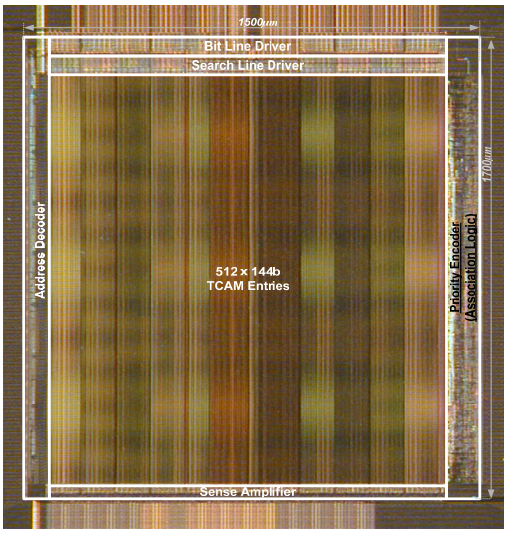

Figure 8.7.7: Die micrograph of the prototype chip implemented in a 1.2V 0.13μm CMOS process.

